Metallic Cover over Wilkinson Power Divider

Introduction

The **Wilkinson power divider** is a rather simple microwave circuit that allows equal splitting the input power to two of the identical output ports. This is achieved by following the design equations relating characteristic impedances of divider branches and the resistor to the port impedances, as indicated in Figure 1. The device can be designed in various technologies but, in this application note, the implementation is in microstrip technology.

The **EM simulation** carried out in the **WIPL-D Pro 3D EM solver** is itself rather simple, regardless the **high operating frequency of 25 GHz and extremely thin substrate** (0.005 mm with Er=3). The influence of a metallic box, typically used to package the divider device, to the divider performance is also examined.

WIPL-D Model of Wilkinson Divider

The general concept of the device is presented in Figure 1. The divider circuit as modeled in WIPL-D Pro 3D EM solver is shown in Figure 2.

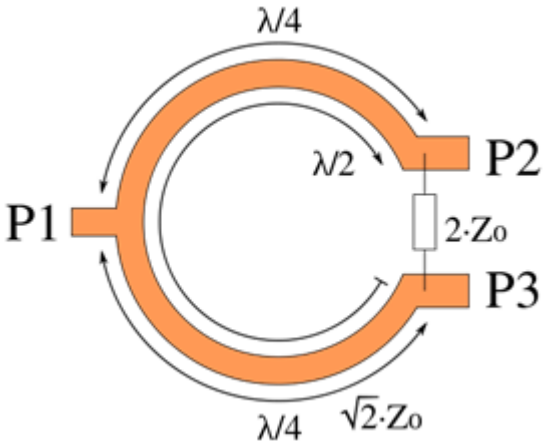

Figure 1. Wilkinson power divider scheme.

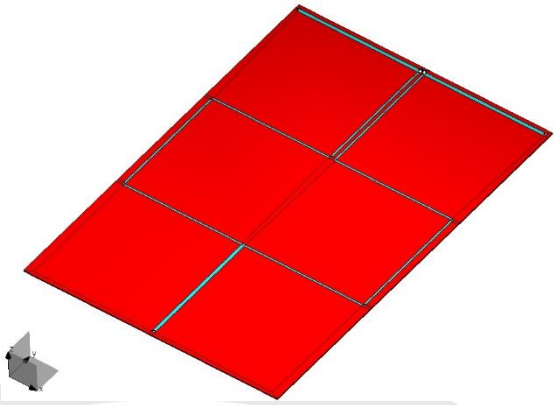

Figure 2. Wilkinson power divider in microstrip technology modeled in WIPL-D Pro.

The model comprises simple microstrip lines and 3 finite ground microstrip ports. Port 1 shown in Figure 1 represents an input port, while ports 2 and 3 also shown in Figure 1 represent output ports. The most efficient way to model microstrip ports in the WIPL-D Pro 3D EM solver is as indicated in Figure 3. Basically, a port is created using two trapezoidal plates with a short/thin wire in between. Both wire ends are connected to metallic quads via triple junctions, which instructs the kernel to consider all three nodes to be in electrical connection. Such feeding mechanism inherently enables **very low reflection loss in the feeder area**.

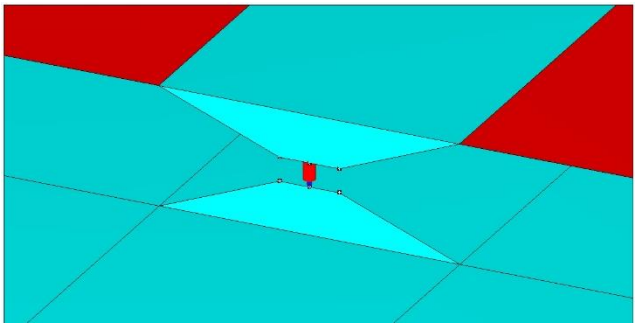

Figure 3. Recommended microstrip feeder in WIPL-D Pro.

The lumped resistor is realized via **concentrated loading**. The resistor construction is quite similar to the one used to create a microstrip feeder (Figure 4).

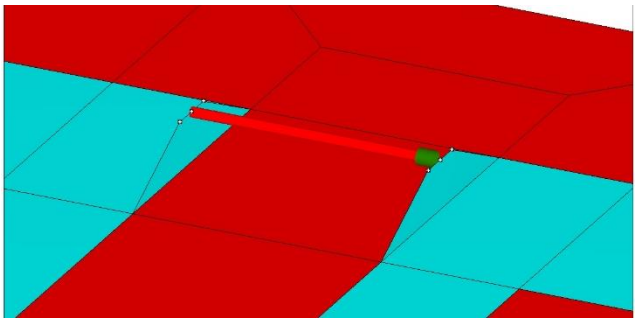

Figure 4. Concentrated loading in WIPL-D Pro.

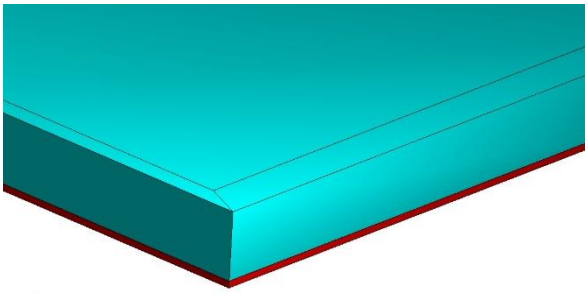

Figure 5. Metallic cover in WIPL-D Pro.

Finally, a metallic box is added to the model of the divider to decrease EM coupling with neighboring devices (Figure 5). The performance of the divider with and without the box is compared in the following figures. The adding of the box can be elegantly

performed using *Copy\Layer* manipulation which only requires grouping plates in one layer.

Simulation Results

The most relevant results include return loss for the first port, coupling between the first and second (or third) port, as well as coupling between the second and third port (Figures 6-8).

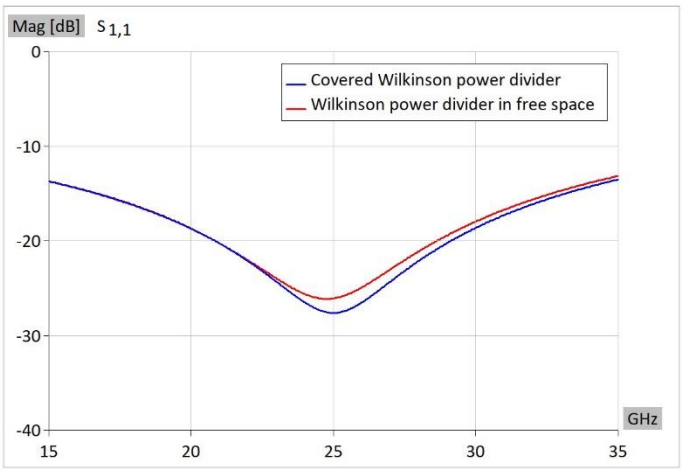

Figure 6. Return loss (port #1).

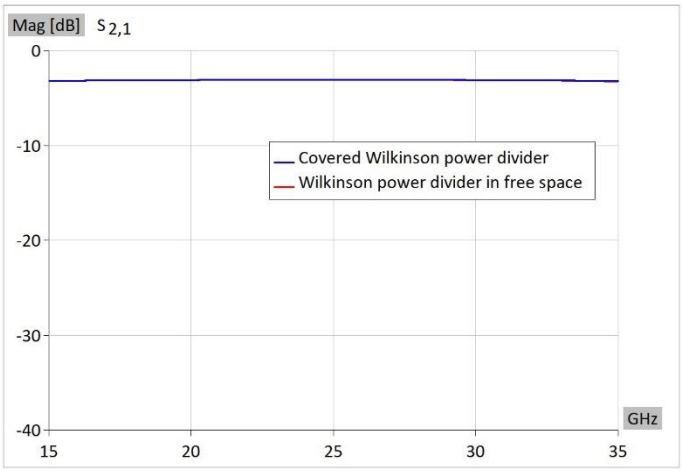

Figure 7. Transmission from port #1 to port #2(3)

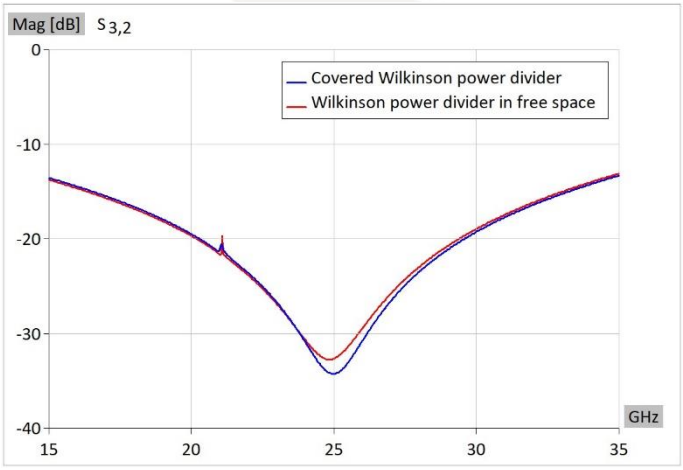

Figure 8. Coupling between ports #2 and #3

The results are as expected:

- Very low return loss for microstrip ports
- Equal power division (-3 dB) between the input and the outputs
- Very good isolation between the output ports
- Rather low influence of adding the metallic cover.

Simulation is performed on **standard desktop PC** with Intel Core i7-7700k CPU at 3.60 GHz. Simulation time per frequency is around **5 seconds** for the model without metal box, while it rises to **8 seconds** when the box is added. Model without the box requires 1,064 unknowns, while the model with the box included requires 1,429 unknowns. Number of unknowns can be halved if the property of divider symmetry is exploited.

Table 1. Number of unknowns and simulation time per frequency.

Model	Number of unknowns	Simulation time per frequency [seconds]
Wilkinson power divider in free space	1,064	5.5
With metallic cover	1,429	8

Simulation times are affected with the presence of a very thin substrate (0.005 mm). The kernel automatically detects very closely spaced layers and increases the simulation parameter named *Integral Accuracy* which in effect increases the simulation time. However, it does not affect the total number of unknowns and the **simulation time remains in the order of several seconds on any modern desktop or laptop PC**. The simulation **results are very accurate with the default simulation settings**, eliminating the need for pursuing the convergence study to establish accurate results.