Bond Wires as Interconnect Technology

Utilization of semiconductor integrated circuits in modern microwave systems has considerably increased in recent times. The trend is the result of the significant technological advances in silicon and silicon-germanium technologies that enabled production of commercially attractive circuits having performance in line with the performance of the traditional monolithic microwave integrated circuits (MMICs) made from GaAs or similar III-V compounds.

A semiconductor bare die must be connected to other circuits comprising a microwave front-end. The traditional way for providing such connections is utilization of bond wires (BW). In short, bond wire interconnect technology uses tiny wires made from gold or aluminium to make connections between a die and a transmission line, or a package pad. The connections are made at elevated temperature by applying ultrasonic energy to attach a wire between desired locations. Dedicated equipment, various types of so-called bonders, are crucial for the process. Bonders provide all of the necessary controls and adjustments for several process parameters that are important to successfully complete delicate interconnecting.

Bond wire interconnections are not ideal. The inductance of the wire together with its capacitance to the ground forms a low pass filter. Therefore, as operating frequency increases, the performance of the interconnections deteriorates. In effect, the overall performance of a circuit integrated within the die together with BWs attached to it may become considerably different from the performance of the bare die alone. This can significantly affect the characteristics of the microwave front end. This application note describes utilization of WIPL-D Microwave design environment for the modeling of two bond wire structures. The models are subsequently utilized in two bare die application scenarios.

Modeling of Bond Wires

The most accurate method to calculate the characteristics of bond wires is electromagnetic (EM) simulation. As bond wires may come in many different shapes, a sufficiently flexible but unified modeling of the wire geometry in EM simulators has been required in order to compare different simulation methods applied to various wire structures. Therefore, a standard for EM modeling of bond wires has emerged - EIA/JEDEC Bond Wire Modeling Standard EIA/JESD59. According to the standard, any wire geometry is modeled with five quantities presented in Fig. 1 – three lengths (h1, h2, d) and two angles (α, β). The standard suggests an approximation of the circular cross section of a wire with an equilateral polygon. A recommended minimum for number of polygon sides is four.

Due to built-in functions for generating various complex objects and powerful symbolic driven geometry modeling in WIPL-D Microwave, the standardized wire geometry can be introduced

easily as a parameterized EM component. The wire body can be created by sweeping a hexagon, modeling a wire cross section, along the parameterized path presented in Fig. 1. In WIPL-D Microwave this requires a single operation, as a possibility to create an object using sweeping a contour along a path is conveniently available within the program through Body of Constant Cross section (BoCC) option. Two wire segments providing horizontal connections at the start and the end (i.e. with non-constant cross section) have been added subsequently in a parametric form. The complete wire model as implemented in the program is presented in Fig. 2.
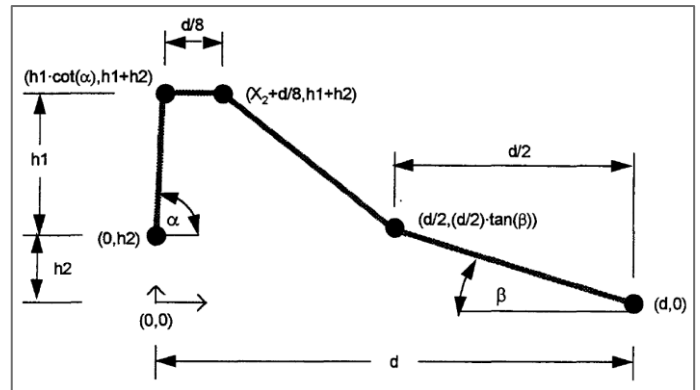

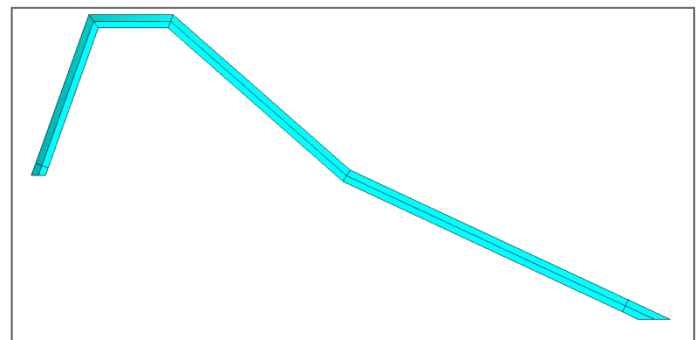**Figure 1. EIA/JEDEC Bond Wire Modeling Standard EIA/JESD59.**

Figure 2. Parameterized WIPL-D model of a Bond Wire conforming with EIA/JESD59 modeling standard.

Single vs. Double Bond Wires

The performance of two frequently used BW structures presented in Fig. 3 is analyzed in the following text. The first one is a simple, single bond wire connection while the second one comprises a parallel connection of two BWs. Both structures have been built around the wire model from Fig. 2.

A real-life example of connecting a commercially available GaAs amplifier die to a microstrip line has been selected as a test vehicle for the comparison of performance between single and double BWs. Input and output connections on the die are provided in a form of a 0.19x0.11 mm sized pad. One end of BW

rests in the middle of the pad located 100 μm from die edge. The die has a thickness of 100 μm, and the bottom of the die is the ground. The microstrip substrate has a relative dielectric constant εr=3.5 and thickness of h0=254 μm. The distance between the die and a microstrip substrate has been set to 200 μm, distance between the microstrip and substrate edges is 100 μm. Second bonding end is located in the middle of 50 Ω microstrip line (550 μm wide), 50 μm from the line end. The wire diameter is 17 μm and the loop height corresponding to h1 from Fig. 1 is 350 μm. The values of the angles are α=80° (at the die) and, β=15° (at the microstrip). Port 1 is located at the die and port 2 is at the microstrip line.
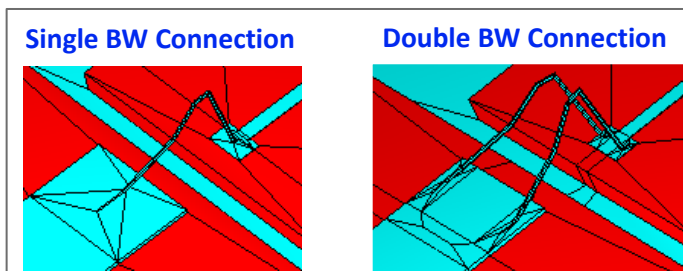

Figure 3. Single and double bond wire connections between a pad and a microstrip line.
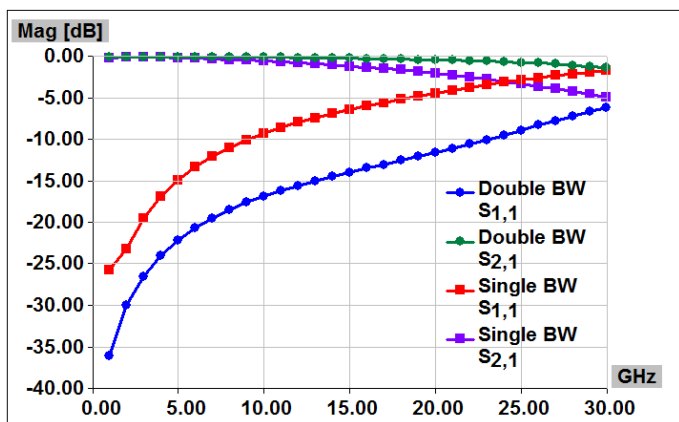

Figure 4. The results of the simulations of two BW structures presented in Fig. 3.

For the double WBs, on the die side, wires are attached 30 μm from the pad edge, while on the microstrip side the wires are located at the corners, 50 μm from each edge.

The results of the simulations of the structures from Fig. 3 are presented in Fig. 4. For single WB, return loss value better than 10 dB is achieved below approximately 10 GHz while the same return loss value is attained bellow approximately 25 GHz for a double BW connection.

It is evident that the performance of the double BW connection is much better than the performance of a single connection as the return loss bandwidth is more than doubled. The improvement is resulting from two effects. The first one is easy to identify as it is simply a consequence of parallel wire connection which, in ideal case, halves the inductance of a single wire. However, due to the mutual inductance between the wires,

the effect of reducing the inductance of the parallel wire connection is less efficient than in the ideal case. The second effect is again related to reducing an inductance, but is not directly related to the properties of the wire. It is linked to the longitudinal microstrip current distribution. As illustrated in Fig. 5, the most of the longitudinal microstrip current is flowing close to the strip edge. When applying a single WB, i.e. when a connection is made in the middle of the strip, a large disturbance of the normal microstrip current distribution is created as the current is injected at the center of the strip, and has to flow from there towards the edges of the strip. This effect creates an inductive discontinuity. However, when two wires are applied at the corners of the strip as described, the inductance arising from this effect is minimized. Microstrip current distribution for both of the structures is presented in Fig. 6. The current distributions have been calculated simply by selecting required calculation options within the program and plotted using versatile graphical interface of WIPL-D Microwave. For the single wire connection, the spike in the current distribution at the location of wire connection indicates significant discontinuity. For the case of double wire connections current distribution plot is smooth indicating that discontinuity effect is minimal.
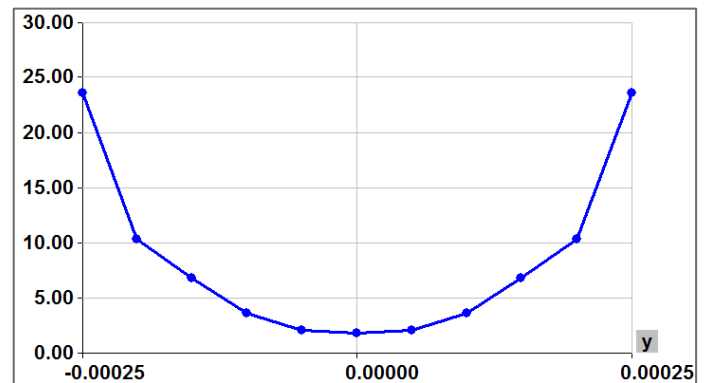

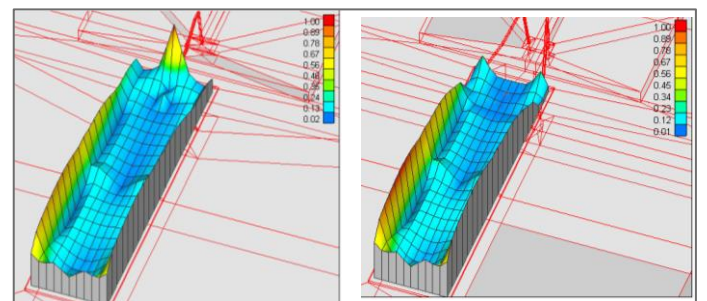**Figure 5. Microstrip longitudinal current distribution across the strip width.**

Figure 6. Current distribution on the microstrip line at 20 GHz for structures presented in Fig. 3.

Connecting a Single LNA Die

In order to compare the influence of two bonding arrangements to the performance of the selected 20 -27 GHz GaAs low noise amplifier (LNA), circuit schematics presented in Fig. 7 have been analyzed. Firstly, a schematic containing only a data set of

measured S parameters probed directly at the die pads (supplied by a manufacturer) has been simulated. The results are plotted in blue in Fig. 8. Secondly, two data blocks containing the results of EM simulations for a single BW structure have been added to the schematics to take into account the effects of bond wires at input and output. The results of the simulation are presented in red in Fig. 8. Finally, a data blocks containing S parameters for single BW structure have been replaced with a data blocks of EM simulated S parameters for a double WB structure. The simulated data are presented in green in Fig. 8.

Comparing the amplifier gain for three of the cases, it can be concluded that single BW case exhibits a gain drop of approximately 3 dB in the whole frequency band 20 -27 GHz with the maximum difference of approximately 5 dB around 22 GHz. On the other hand, within the same bandwidth, the gain calculated for double WB case almost exactly follows the measured gain curve. Regarding the return loss curves, neither of the wire bonds structures closely follows the curves as measured directly on the die. However, the values of approximately 10 dB obtained with the double BW structure are adequate for most of the practical situations while the values smaller than 5 dB, obtained for single BW, are not acceptable.
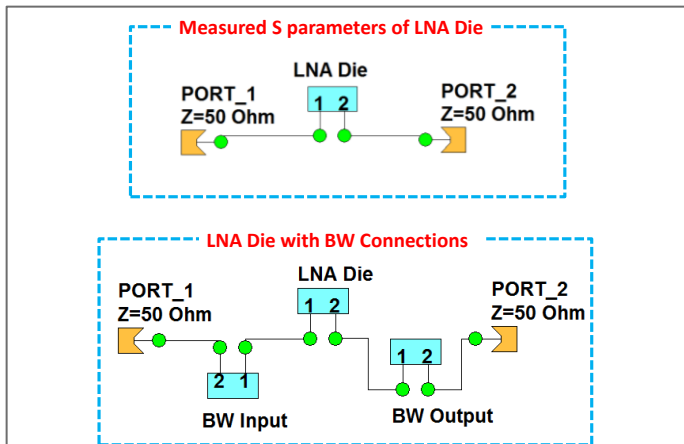

Figure 7. Schematics used to simulate S parameters of LNA bare die and bonded LNA.

The results presented in Fig. 8 indicate that the influence of BWs to the performance of the die can be significant. Actually, the deterioration of the performance of the LNA die when bonded with a single BW at each end is substantial and makes the bonded die practically unusable for any application. It seems like the utilization of double BW structure results in overall good performance. However, this conclusion has to be considered very carefully.

The values of S11 around 10 dB in the whole operating bandwidth are good enough to apply the amplifier as a gain block anywhere within a system, but should be carefully examined for the case of an input LNA amplifier. The input internal matching of the LNA located within the die normally transforms the input impedance (50 Ω) to selected impedance at the transistor input terminal which provides desired noise figure of the whole

amplifier. The simulated values of the return loss for the bonded amplifier presented in Fig. 8 are considerably different from values measured directly on the die. Accordingly, the noise performance associated with optimal noise match at the input is not guaranteed. It means that the amplifier considered in this example, even when bonded with double BWs, may not behave as expected. In the circumstances described above, a noise figure of a receiver chain with the amplifier used as a first stage may not be optimal.
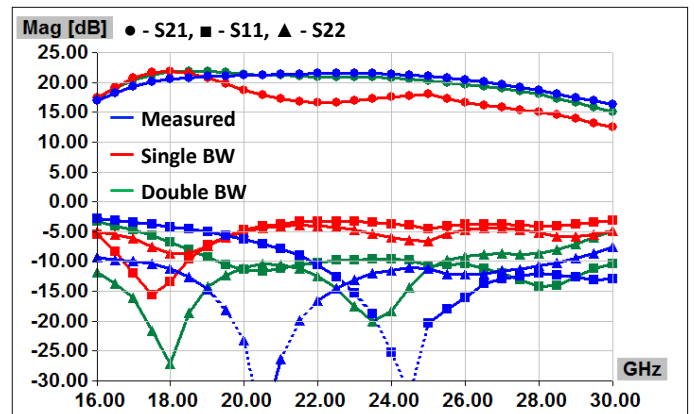

Figure 8. Simulated S parameters of bonded amplifier from Fig. 7 when single and double BWs are applied.

Cascading PA and PA Driver Dies

In the previous section it has been explained that BWs can degrade the performance of a bare die to the extent that it becomes unusable. Cascading several dies, which is quite common when using monolith microwave integrated circuits (MMICs) to build a microwave front end of a system, brings in additional effects.

To illustrate the effects, a previously described amplifier die is used as a driver amplifier for a PA die available from the same manufacturer (with the same semiconductor material, die thickness and pad size). The interconnection between the amplifiers is designed as a piece of a 50 Ω microstrip line with bond wires attached at both sides. To establish a baseline result, direct (ideal) connection of the two dies has been simulated first. Then the schematic is modified by inserting four BW and a length of interconnecting microstrip line as shown in Fig. 9. The length of microstrip line has been varied from L=0 (where only a minimum length of the line necessary to make BW connection is included in each BW data block) to L=3 λ/8 in four steps. Wavelength λ is microstrip wavelength at 23 GHz.
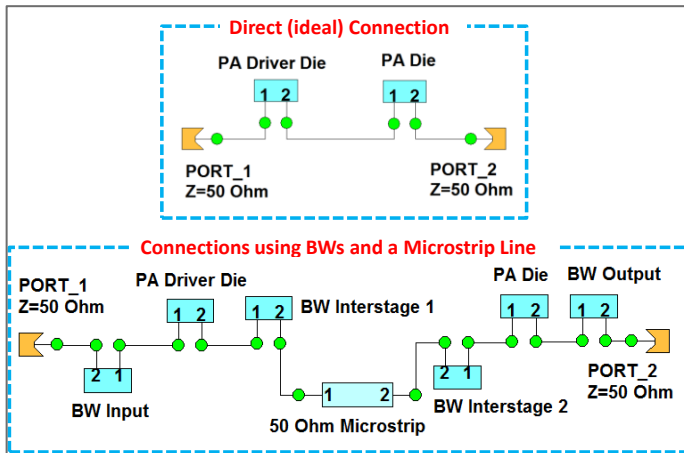
Figure 9. Schematics used to simulate S parameters of cascaded PA driver and PA bare dies.
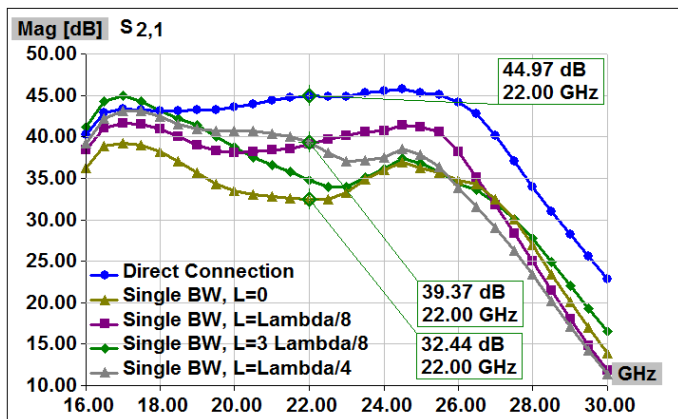

Figure 10. Simulated S parameters of bonded two stage amplifier from Fig. 9 when single BWs are applied.
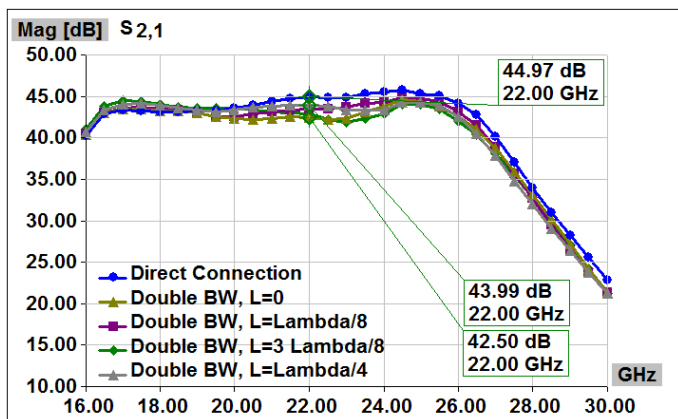

Figure 11. Simulated S parameters of bonded two stage amplifier from Fig. 9 when double BWs are applied.

Simulated combined gain of the two stage amplifier is presented in Fig. 10 for the case where single BWs have been used to make the connections, and in Fig. 11 where double BWs have been used. For the case of single BWs, the variation of the gain when a length of the interconnecting line is varied is approximately 7 dB. That is a significant variation, especially when having in mind that the maximum of the gain is more than 5 dB lower than for the case of ideal connection. In other words, for the worst case

occurring when L=0, two stage amplifier gain is 12.5 dB lower than for the case of ideal connections.

The maximum gain variations are much smaller when double BWs are used. This is obvious from Fig. 11 where a variation of approximately 2.5 dB from the baseline design can be seen.

The example presented indicates that in a cascade of several bare dies, performance of the interconnect technology applied becomes of crucial importance. Multiple reflections between several connections can cause ripples in gain, return loss or group delay that can have deleterious effect of the system performance. Generally, for the system design involving bonded bare dies, it is not always appropriate to simply sum the gains of cascaded stages and subtract the insertion losses of the interconnects. To obtain a good approximation with this approach, the return loss of the interconnects should be in the range of 15 dB. More complete and reliable approach will involve electromagnetic analysis, experimental testing and optimization of interconnects to ensure their minimal impact to the system performance and optimal use of each die within the system.

Conclusion

Accurate modeling of the bonding wires is essential to successfully utilize semiconductor bare dies and achieve a large scale of integration of modern microwave front ends. WIPL-D Microwave provides a complete design environment where electromagnetic and circuit simulation can be efficiently applied to examine the influence of interconnects to the performance of an integrated system.

The limitations of the single wire bonds regarding the relatively narrow return loss bandwidth have been illustrated through the analysis of performance degradation of an amplifier. The improvement of the characteristics when double wire bonds are utilized are presented and the mechanizm of the improvement explained. The importance of optimizing the return loss of the interconnects is emphasized showing deleterious effect of multiple reflections to the performance of a multistage amplifier.

The selected examples concentrate on the applications in the frequency range around 24 GHz. However, as the operating frequency goes higher, the effects of interconnects become more severe and some means of compensation of bond wire connections described in the literature must be utilized to keep the return loss at reasonable values. If these are not adequate for the particular situation on hand, a different interconnect technology, such as flip chip of micro ball grid array (μBGA), has to be considered.